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*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L1 710/100,300,305;365,63,189.01,189.05,230.01,230.08,205;713/501;711/100,103;712/33;327/266

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### Search History

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*DB=PGPB,USPT,USOC; PLUR=YES; OP=OR*

L3    l1 and L2

L2    "helper flip flop" or "helper flip-flop"

L1    710/100,300,305;365,63,189.01,189.05,230.01,230.08,205;713/501;711/100,103;712/33;327/266

END OF SEARCH HISTORY

EAST - [Untitled1:1]

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L1: (3737) (first adj1 bus) same (second adj1 bus)

L2: (19) 11 same speed same

L3: (3) 12 and ("flip-flop")

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UDC

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	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments	Error Definition	Err
1	BRS	L1	3737	(first adj1 bus) same (second adj1 bus)	USPAT	2005/01/19 15:59			
2	BRS	L2	19	11 same speed same width	USPAT	2005/01/19 15:59			
3	BRS	L3	3	12 and ("flip-flop" or "flip flop")	USPAT	2005/01/19 16:00			

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EAST - [Untitled1:1]

EAST - [Untitled1:1]

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L2: (19) 11 same speed same

L3: (3) 12 and ("flip-flop")

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12 and ("flip-flop" or "flip flop")

BRS form

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Image

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	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	R
1	<input type="checkbox"/>	<input type="checkbox"/>	US 5710892 A	19980120	9	System and method for asynchronous dual bus	710/307	326/46; 703/27;	
2	<input type="checkbox"/>	<input type="checkbox"/>	US 5524270 A	19960604	8	System for transferring data between asynchronous data	710/310	375/354; 375/357;	
3	<input type="checkbox"/>	<input type="checkbox"/>	US 5406525 A	19950411	18	Configurable SRAM and method for providing the same	365/230.02	365/189.02; 365/230.03	

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You may refine your search by editing the current search expression or entering a new one in the text box.


☐ Check to search within this result set
**Results Key:**
**JNL** = Journal or Magazine   **CNF** = Conference   **STD** = Standard

**1 A low power and high speed data transfer scheme with asynchronous compressed pulse width modulation for AS-memory**
*Yamauchi, T.; Morooka, Y.; Ozaki, H.;*

VLSI Circuits, 1995. Digest of Technical Papers., 1995 Symposium on , 8-10 J 1995

Pages:27 - 28

[\[Abstract\]](#)   [\[PDF Full-Text \(188 KB\)\]](#)   IEEE CNF

**2 A low power and high speed data transfer scheme with asynchronous compressed pulse width modulation for AS-Memory**
*Yamauchi, T.; Morooka, Y.; Ozaki, H.;*

Solid-State Circuits, IEEE Journal of , Volume: 31 , Issue: 4 , April 1996

Pages:523 - 530

[\[Abstract\]](#)   [\[PDF Full-Text \(1128 KB\)\]](#)   IEEE JNL


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## A low power and high speed data transfer scheme with asynchronous compressed pulse width modulation for AS-memory

Yamauchi, T. Morooka, Y. Ozaki, H.

ULSI Lab., Mitsubishi Electr. Corp., Itami, Japan;

*This paper appears in: VLSI Circuits, 1995. Digest of Technical Papers., 1995 Symposium on*

Meeting Date: 06/08/1995 - 06/10/1995

Publication Date: 8-10 June 1995

Location: Kyoto Japan

On page(s): 27 - 28

Reference Cited: 2

Inspec Accession Number: 5212052

### Abstract:

We propose a high speed and low power data transfer scheme for the wide internal data bus of an AS-Memory using the asynchronous compressed pulse width modulation (AC-PWM) technique and an automatic gain controlled (AGC) amplifier. The maximum bit rate per bus of AC-PWM increases by 1.2 times that of the conventional 100MHz data bus. The AGC amplifier achieves a fast data output while reducing by 1/3 the standby current. The proposed architecture is a key advance in the future development of AS-

Memories

**Index Terms:**

[application specific integrated circuits](#) [automatic gain control](#) [differential amplifiers](#) [integrated memory circuits](#) [memory architecture](#) [pulse width modulation](#) [system buses](#) [AC-PWM](#) [AGC amplifier](#) [AS-memory](#) [asynchronous compressed pulse width modulation](#) [automatic gain controlled amplifier](#) [internal data bus](#) [low power high speed data transfer](#)

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protocol comprises an asynchronous request signal from the first bus requesting a data transfer and an asynchronous reply signal from the second bus indicating that data has been sent or is available.

Brief Summary Text - BSTX (16):

To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described, the invention provides for a bus interface system in communication with first and second computer components, comprising a first bus associated with the first component, the first bus having a first characteristic speed, data width, and protocol; a second bus associated with the second component, the second bus having a second characteristic speed, data width, and protocol, wherein at least one of the second characteristics is different from the first characteristics; a first state machine communicating with the first bus; a second state machine communicating with the second bus; and data storage means associated with the first and second buses, the first and second state machines being in selective communication using an asynchronous handshaking protocol, whereby data is transferred between the first and second buses.

Brief Summary Text - BSTX (17):

In another aspect, the invention provides for a method of asynchronous dual bus conversion using first and second state machines for a computer system having a first bus having a first characteristic speed, data width, and protocol, and a second bus having a second characteristic speed, data width, and protocol, wherein at least one of the second characteristics is different than the first characteristics, the method comprising the steps of: storing data to be transferred in a data storage means; initiating an asynchronous request signal by the first state machine in communication with the first bus, having a format comprising the first characteristics, thereby requesting that data in the data storage means be transferred; and initiating an asynchronous reply signal by the second state machine in communication with the second bus, having a format comprising the second characteristics, thereby signalling that the data has been sent or is available.

Drawing Description Text - DRTX (6):

FIG. 4 is logic diagram of clocked flip-flops for use with the asynchronous signals of the present invention.

Detailed Description Text - DETX (17):

One way to eliminate the metastability problem is through the use of clocked D flip-flops. In a D flip-flop, the output is equal to the value of the stored state inside the element. The output of a flip-flop changes only on a clock edge, and the flip-flop may be designed for either a rising (positive) or



US005710892A

**United States Patent** [19]

Goodnow et al.

[11] Patent Number **5,710,892**[45] Date of Patent: **Jan. 20, 1998****[54] SYSTEM AND METHOD FOR ASYNCHRONOUS DUAL BUS CONVERSION USING DOUBLE STATE MACHINES**

[72] Inventors: Kenneth Joseph Goodnow, Essex Jct.; Dana John Tryggestad, Huntington, both of Vt.

[73] Assignee: International Business Machines Corporation, Armonk, N.Y.

[21] Appl. No.: 884,847

[22] Filed: Jul. 19, 1995

[31] Int. Cl.<sup>6</sup> G06F 13/00; G06F 13/04

[32] U.S. Cl. 395/347; 395/308; 395/327; 395/346

[33] Field of Search 395/304, 307, 395/303, 307; 395/346

**[36] References Cited****U.S. PATENT DOCUMENTS**

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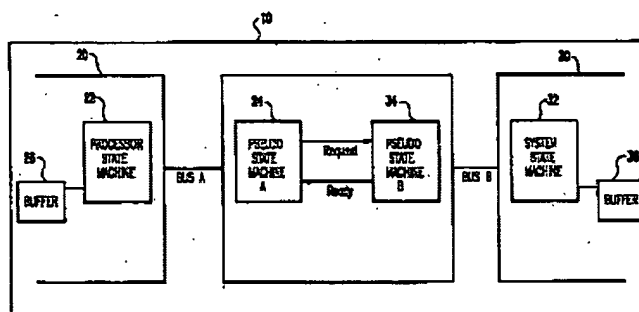
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5,549,025 10/1996 Ansel et al. 395/325

Primary Examiner—Jack B. Harvey  
Assistant Examiner—Jeffrey E. Soto  
Attorney, Agent or Firm—Whittem, Curtis, Whittem & McCain; Mark R. Chastelain

**[57] ABSTRACT**

A bus interface system and method for communication between different computer components having buses with different speeds, data widths, or protocols. A first state machine communicates with the first bus and a second state machine communicates with the second bus. Each of the buses communicates with a data storage device. The first and second state machines are in selective communication using an asynchronous handshaking protocol, whereby data is transferred between said first and second buses. The handshaking protocol comprises an asynchronous request signal from the first bus requesting a data transfer and an asynchronous reply signal from the second bus indicating that data has been sent or is available.

14 Claims, 4 Drawing Sheets



US-PAT-NO: 5406525  
DOCUMENT-IDENTIFIER: US 5406525 A  
TITLE: Configurable SRAM and method for providing the same

----- KWIC -----

Abstract Text - ABTX (1):

A configurable SRAM (21) is provided that is full diffused for increased speed and density and configurable for different word widths. Configuration signals are applied to control logic (28) for selecting a word width. The word width is smaller than or equal to a bit string of configurable SRAM (21). In a write operation, data input registers store and couple a word to a second bus. A shifter (27) receives the word from the second bus and shifts the bit locations of the word. A multiplexer (26) couples the shifted word to a first bus where write circuitry of read/write circuitry (24) writes the word to a selected bit string of a memory array (22) without affecting other bits of the selected bit string.

Brief Summary Text - BSTX (4):

Gate arrays are designed to be extremely efficient at forming simple logic blocks commonly used in digital circuits. For example, NAND gates, NOR gates, inverters, and flip flops. Efficiency of metallization (or routing) of a gate array is measured by the total number of transistors used versus the total number of transistors in the gate array. Circuits formed with the simple logic blocks described above typically achieve efficiencies of approximately 80 percent or less.

## United States Patent [19]

Nicholas

[11] Patent Number: 5,406,525

[45] Date of Patent: Apr. 11, 1995

## [34] CONFIGURABLE SRAM AND METHOD FOR PROVIDING THE SAME

[75] Inventor: James W. Nicholas, Gilbert, Ariz.

[73] Assignee: Motorola, Inc., Schaumburg, Ill.

[21] Appl. No.: 254,848

[22] Filed: Jan. 6, 1994

[31] Int. Cl. G11C 12/02; H03K 19/177

[32] U.S. Cl. 362/228.02; 362/189.02;

362/230.02; 362/230.03

[33] Field of Search 362/230.01, 230.02,

362/230.03, 230.03, 189.02, 189.04

[36] Reference Cited

U.S. PATENT DOCUMENTS

4,115,178 8/1994 Schick 362/230.02

Primary Examiner—Terry W. Peas

Attorney Agent or Firm—Gary W. Hochstadt

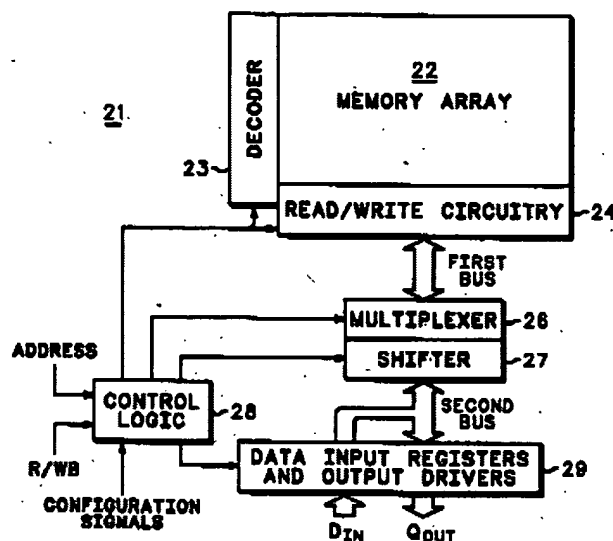
[37] ABSTRACT

A configurable SRAM (21) is provided that is full diffused for increased speed and density and configurable

for different word widths. Configuration signals are applied to control logic (28) for selecting a word width. The word width is smaller than or equal to a bit string of configurable SRAM (21). In a write operation, data input registers store and couple a word to a second bus. A shifter (27) receives the word from the second bus and shifts the bit locations of the word. A multiplexer (26) couples the shifted word to a first bus where write circuitry of read/write circuitry (24) writes the word to a selected bit string of a memory array (22) without affecting other bits of the selected bit string.

In a read operation, a selected bit string is provided from the memory array (22) to read circuitry. The read circuitry provides the selected bit string to the first bus. The multiplexer (26) couples a word from the selected bit string to the shifter (27). The shifter (27) shifts the bits of the word adjacent to one another on the second bus. Output drivers of the data input registers and output drivers (29) provide the word to other circuitry.

18 Claims, 9 Drawing Sheets



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L7: Entry 68 of 69

File: USPT

Jun 28, 1994

DOCUMENT-IDENTIFIER: US 5325330 A

TITLE: Memory circuit with foreshortened data output signal

Drawing Description Text (10):

FIG. 9 is a schematic diagram of a helper flip flop included in an alternate embodiment of the sense amplifiers of the memory device shown in FIG. 1.

Detailed Description Text (19):

Prior to coupling to the data output buffer, the signals on the IO lines are amplified. Two circuits for such amplification will be discussed. The first is called a DC sense amplifier and is similar to an analog differential amplifier (FIG. 5). The second is a bistable circuit called a helper flip flop (FIG. 9).

Detailed Description Text (41):

FIG. 9 is a schematic diagram of helper flip flop 500 included in an alternate embodiment of sense amplifiers 22 shown in FIG. 1. Helper flip flop 500 is used in place of DC sense amplifier 270 shown in FIG. 5. DC sense amplifier 270, in some applications will operate at increased power dissipation compared to helper flip flop 500.

Detailed Description Text (42):

Outputs of helper flip flop 500 are coupled to global IO lines 128 and 130 shown on FIG. 3 or, alternatively, lines 462 and 464 shown on FIG. 8. FET 510 equilibrates lines 520 and 522. Thus, at the initiation of a read operation, GIO1 and GIO2 have matching signal levels. IO signals 262 and 266 representing data read from an addressed memory cell (shown also on FIG. 4) are gated through FETs 502 and 504 respectively at a time determined by a fixed delay from the falling edge of RAS\*. Global IO signals GIO1 and GIO2 on lines 520 and 522 separate as soon as cross-coupled FETs 506 and 508 attain a stable state matching the state of IO lines 262 and 266.

Detailed Description Text (43):

As described above, helper flip flop 500 depends for operation on delay circuitry driven from RAS\*. The access time of a memory device employing helper flip flop 500 depends on a predetermined worst case calculation of when data on IO lines 262 and 266 is valid from any addressed cell. In contrast, in a memory device employing DC sense amplifier 270, the access time depends on a measurable condition of validity signified directly by IO lines 262 and 266 for the particular cell addressed to be read.

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L7: Entry 1 of 69

File: PGPB

Sep 9, 2004

PGPUB-DOCUMENT-NUMBER: 20040177208  
PGPUB-FILING-TYPE: new  
DOCUMENT-IDENTIFIER: US 20040177208 A1

TITLE: Reduced data line pre-fetch scheme

PUBLICATION-DATE: September 9, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Merritt, Todd A.	Boise	ID	US	
Morgan, Donald M.	Meridian	ID	US	

APPL-NO: 10/ 773074    [\[PALM\]](#)  
DATE FILED: February 5, 2004

## RELATED-US-APPL-DATA:

Application 10/773074 is a division-of US application 09/652390, filed August 31, 2000, US Patent No. 6704828

INT-CL: [07] [G06 F 13/14](#)

US-CL-PUBLISHED: 710/305

US-CL-CURRENT: [710/305](#)

REPRESENTATIVE-FIGURES: 2

## ABSTRACT:

A data amplifier configured to allow for fewer data lines and/or increased processing speeds. Specifically, multiple helper flip-flops are used to prefetch data in a data amplifier. The helper flip-flops are configured to latch one or two of the data bits from a 4-bit prefetch in an alternating periodic fashion, thereby necessitating fewer data lines. Alternatively, the number of data lines can be maintained and faster bus processing speeds may be realized.

## CROSS-REFERENCE TO RELATED APPLICATIONS

[0001] The present application is a divisional of U.S. application Ser. No. 09/652,390, filed on Aug. 31, 2000.

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L7: Entry 68 of 69

File: USPT

Jun 28, 1994

DOCUMENT-IDENTIFIER: US 5325330 A

TITLE: Memory circuit with foreshortened data output signal

Drawing Description Text (10):

FIG. 9 is a schematic diagram of a helper flip flop included in an alternate embodiment of the sense amplifiers of the memory device shown in FIG. 1.

Detailed Description Text (19):

Prior to coupling to the data output buffer, the signals on the IO lines are amplified. Two circuits for such amplification will be discussed. The first is called a DC sense amplifier and is similar to an analog differential amplifier (FIG. 5). The second is a bistable circuit called a helper flip flop (FIG. 9).

Detailed Description Text (41):

FIG. 9 is a schematic diagram of helper flip flop 500 included in an alternate embodiment of sense amplifiers 22 shown in FIG. 1. Helper flip flop 500 is used in place of DC sense amplifier 270 shown in FIG. 5. DC sense amplifier 270, in some applications will operate at increased power dissipation compared to helper flip flop 500.

Detailed Description Text (42):

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L7: Entry 68 of 69

File: USPT

Jun 28, 1994

US-PAT-NO: 5325330

DOCUMENT-IDENTIFIER: US 5325330 A

TITLE: Memory circuit with foreshortened data output signal

DATE-ISSUED: June 28, 1994

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Morgan; Donald M.	Boise	ID		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Semiconductor, Inc.	Boise	ID			02

APPL-NO: 08/ 017095   [\[PALM\]](#)

DATE FILED: February 11, 1993

INT-CL: [05] G11C 7/00

US-CL-ISSUED: 365/189.05; 365/189.31, 365/203, 365/230.01

US-CL-CURRENT: 365/189.05; 365/189.01, 365/203, 365/230.01

FIELD-OF-SEARCH: 365/189.05, 365/233.5, 365/230.08, 365/230.06, 365/189.01, 365/205, 365/189.11, 365/203

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<input type="checkbox"/>	<u>5245573</u>	September 1993	Nakaoka	365/189.05



ART-UNIT: 251

PRIMARY-EXAMINER: LaRoche; Eugene R.

ASSISTANT-EXAMINER: Nguyen; Tan

ATTY-AGENT-FIRM: Bachand; William R.

ABSTRACT:

A memory device output buffer circuit provides an output data signal only when data is valid. According to the present invention, the circuit for a memory read function provides a pair of signals equilibrated prior to each read operation. Data is valid when the signals are complementary. For a tristate output, the complementary condition enables the output buffer. In a semiconductor dynamic random access memory (DRAM) connectable to a bidirectional data bus, the three-state output buffer of the present invention is not enabled during a read operation until data is valid. Spurious output data signals are prevented from consuming power. As an additional benefit, the bus is not dedicated to the memory when valid data is not yet available.

20 Claims, 9 Drawing figures

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L10: Entry 11 of 18

File: USPT

Jul 2, 2002

DOCUMENT-IDENTIFIER: US 6414904 B2

TITLE: Two channel memory system having shared control and address bus and memory modules used therefor

Abstract Text (1):

A memory system, which can improve the operation speed of a data bus and is suitable for widening bandwidth by extending the width of the data bus, and memory modules used for the memory system are provided. In the memory system, data buses of a first channel and data buses of a second channel are extended from a memory controller and are arranged on the left and right of a common control and address bus, respectively. Memory modules of a first group are loaded in the data buses of the first channel and memory modules of a second group are loaded in the data buses of the second channel. Also, in the memory system, the memory modules share the common control and address bus positioned in the center. Also, the memory modules are arranged so that some parts of the memory modules overlap each other and that the memory modules of the first group and the memory modules of the second group cross each other. Each of the memory modules includes a plurality of memory devices mounted on the memory module, a signal input and output portion positioned on a side of the memory module, the signal input and output portion for connecting the memory module to a connector on a system board, a buffer mounted on the memory module, and a control and address bus connected between the signal input and output portion and the buffer. The memory devices are sequentially connected to the output line of the buffer so that a signal that passed through the control and address bus is input to the respective memory devices at time intervals through the buffer.

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L10: Entry 11 of 18

File: USPT

Jul 2, 2002

US-PAT-NO: 6414904

DOCUMENT-IDENTIFIER: US 6414904 B2

TITLE: Two channel memory system having shared control and address bus and memory modules used therefor

DATE-ISSUED: July 2, 2002

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
So; Byung-se	Sungnam			KR
Park; Myun-joo	Incheon			KR
Lee; Sang-won	Gunpo			KR

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Samsung Electronics Co., Ltd.				KR	03

APPL-NO: 09/ 777547 [\[PALM\]](#)

DATE FILED: February 6, 2001

## FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
KR	00-37399	June 30, 2000

INT-CL: [07] [G11 C 8/00](#)

US-CL-ISSUED: 365/239; 365/189.04, 711/127

US-CL-CURRENT: [365/239](#); [365/189.04](#), [711/127](#)

FIELD-OF-SEARCH: 365/51, 365/63, 365/230.05, 365/189.04, 365/189.08, 365/239, 365/230.09, 711/5, 711/127

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<a href="#">5367632</a>	November 1994	Bowen et al.	395/194
<input type="checkbox"/>	<a href="#">5479624</a>	December 1995	Lee	395/401
<input type="checkbox"/>	<a href="#">5490253</a>	February 1996	Laha et al.	395/304

<input type="checkbox"/>	<u>5860080</u>	January 1999	James et al.	711/4
<input type="checkbox"/>	<u>6016282</u>	January 2000	Keeth	365/233
<input type="checkbox"/>	<u>6128748</u>	October 2000	MacWilliams et al.	713/401
<input type="checkbox"/>	<u>6334159</u>	December 2001	Haupt	710/6

ART-UNIT: 2824

PRIMARY-EXAMINER: Elms; Richard

ASSISTANT-EXAMINER: Nguyen; Hien

ATTY-AGENT-FIRM: Mills & Onello LLP

ABSTRACT:

A memory system, which can improve the operation speed of a data bus and is suitable for widening bandwidth by extending the width of the data bus, and memory modules used for the memory system are provided. In the memory system, data buses of a first channel and data buses of a second channel are extended from a memory controller and are arranged on the left and right of a common control and address bus, respectively. Memory modules of a first group are loaded in the data buses of the first channel and memory modules of a second group are loaded in the data buses of the second channel. Also, in the memory system, the memory modules share the common control and address bus positioned in the center. Also, the memory modules are arranged so that some parts of the memory modules overlap each other and that the memory modules of the first group and the memory modules of the second group cross each other. Each of the memory modules includes a plurality of memory devices mounted on the memory module, a signal input and output portion positioned on a side of the memory module, the signal input and output portion for connecting the memory module to a connector on a system board, a buffer mounted on the memory module, and a control and address bus connected between the signal input and output portion and the buffer. The memory devices are sequentially connected to the output line of the buffer so that a signal that passed through the control and address bus is input to the respective memory devices at time intervals through the buffer.

24 Claims, 5 Drawing figures

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L20: Entry 26 of 30

File: USPT

Sep 24, 1996

DOCUMENT-IDENTIFIER: US 5559969 A

**\*\* See image for Certificate of Correction \*\***

TITLE: Method and apparatus for efficiently interfacing variable width data streams to a fixed width memory

Brief Summary Text (22):

A number of memory devices may be coupled together via a second bus. The second bus may operate at a lower speed than the first bus such that slower memory accesses may be made over the second bus. As stated above, typical memory devices may not operate at the same speed as high speed processor devices. In the exemplary embodiment, the first bus may operate at twice the frequency of the second bus. To compensate for this frequency differential, it is contemplated that the second bus may have a data width that is twice as wide as the first bus. The significance of the speed/width relationship between the first bus and the second bus will be discussed further infra. It is contemplated that other speed/width ratios fall within the scope of the present invention.

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L20: Entry 26 of 30

File: USPT

Sep 24, 1996

US-PAT-NO: 5559969

DOCUMENT-IDENTIFIER: US 5559969 A

**\*\* See image for [Certificate of Correction](#) \*\***

TITLE: Method and apparatus for efficiently interfacing variable width data streams  
to a fixed width memory

DATE-ISSUED: September 24, 1996

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Jennings; Kevin F.	Noyi	MI		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Unisys Corporation	Blue Bell	PA			02

APPL-NO: 08/ 287880   [\[PALM\]](#)

DATE FILED: August 9, 1994

## PARENT-CASE:

CROSS REFERENCE TO CO-PENDING APPLICATIONS The present application is related to U.S. patent application Ser. No. 08/287,878, filed Aug. 9, 1994, entitled "Method and Apparatus for High Speed Efficient Bi-Directional Communication Between Multiple Processors Over a Common Bus", and U.S. patent application Ser. No. 08/287,879, filed Aug. 9, 1994, now U.S. Pat. No. 5,517,504, entitled "Method and Apparatus for High-Speed Implementation of Scaling, Dithering, and Data Remapping Operations with a Single Processor", both assigned to the assignee of the present invention and both incorporated herein by reference.

INT-CL: [06] [G06 F 13/38](#)

US-CL-ISSUED: 395/307; 395/306

US-CL-CURRENT: [710/307](#)

FIELD-OF-SEARCH: 395/307, 395/306

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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PAT-NO

ISSUE-DATE

PATENTEE-NAME

US-CL

☐[4309754](#)

January 1982

Dinwiddie, Jr.

395/307

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<input type="checkbox"/>	<u>4595911</u>	June 1986	Kregness et al.	340/347
<input type="checkbox"/>	<u>4716527</u>	December 1987	Graciotti	395/307
<input type="checkbox"/>	<u>4860198</u>	August 1989	Takenaka	395/307
<input type="checkbox"/>	<u>4878166</u>	October 1989	Johnson et al.	395/307
<input type="checkbox"/>	<u>5195185</u>	March 1993	Marenin	395/325
<input type="checkbox"/>	<u>5202966</u>	April 1993	Woodson	395/325
<input type="checkbox"/>	<u>5255374</u>	October 1993	Aldereguia et al.	395/307
<input type="checkbox"/>	<u>5255375</u>	October 1993	Crook et al.	395/325
<input type="checkbox"/>	<u>5255378</u>	October 1993	Crawford et al.	395/307
<input type="checkbox"/>	<u>5388227</u>	February 1995	McFarland	395/307

ART-UNIT: 235

PRIMARY-EXAMINER: Harvey; Jack B.

ASSISTANT-EXAMINER: Wiley; David A.

ATTY-AGENT-FIRM: Nawrocki, Rooney & Sivertson, P.A.

ABSTRACT:

An apparatus for and method of providing a system whereby a number of processors may communicate with a memory device and wherein the memory device may operate at a slower speed without substantially reducing the band pass of the computer system. Further, one or more of the processors may have a different data word width from the other processors and from the memory device. The present invention may minimize the amount of wasted memory bits contained therein by concatenating data words such that the resulting data word substantially matches the word width of the memory device. The present invention further allows predefined portions of a data word to be placed in an order and concatenated with predefined portions of the same data word or with predefined portions of other data words. A number of predetermined formats define the selection and the order that the predefined portions may be placed. Various formats are contemplated and are described herein.

62 Claims, 11 Drawing figures

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☐ 1. Document ID: US 20040177208 A1

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L3: Entry 1 of 2

File: PGPB

Sep 9, 2004

PGPUB-DOCUMENT-NUMBER: 20040177208

PGPUB-FILING-TYPE: new

DOCUMENT-IDENTIFIER: US 20040177208 A1

TITLE: Reduced data line pre-fetch scheme

PUBLICATION-DATE: September 9, 2004

INVENTOR-INFORMATION:

NAME	CITY	STATE	COUNTRY	RULE-47
Merritt, Todd A.	Boise	ID	US	
Morgan, Donald M.	Meridian	ID	US	

US-CL-CURRENT: 710/305

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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☐ 2. Document ID: US 6704828 B1

L3: Entry 2 of 2

File: USPT

Mar 9, 2004

US-PAT-NO: 6704828

DOCUMENT-IDENTIFIER: US 6704828 B1

TITLE: System and method for implementing data pre-fetch having reduced data lines and/or higher data rates

Full	Title	Citation	Front	Review	Classification	Date	Reference	Sequences	Attachments	Claims	KWIC	Draw. De
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L1: Entry 1 of 1

File: USPT

Mar 9, 2004

US-PAT-NO: 6704828

DOCUMENT-IDENTIFIER: US 6704828 B1

TITLE: System and method for implementing data pre-fetch having reduced data lines and/or higher data rates

DATE-ISSUED: March 9, 2004

## INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Merritt; Todd A.	Boise	ID		
Morgan; Donald M.	Meridian	ID		

## ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Micron Technology, Inc.	Boise	ID			02

APPL-NO: 09/ 652390 [PALM]

DATE FILED: August 31, 2000

INT-CL: [07] G06 F 13/38, G06 F 13/40, G06 F 12/00, G11 C 5/06

US-CL-ISSUED: 710/305; 710/300, 711/100, 712/33, 365/63

US-CL-CURRENT: 710/305; 365/63, 710/300, 711/100, 712/33

FIELD-OF-SEARCH: 710/100, 710/300, 710/305, 365/63, 365/189.01, 365/230.01, 365/230.08, 365/205, 330/3, 713/501, 711/100, 711/103, 712/33, 327/266, 327/287

PRIOR-ART-DISCLOSED:

## U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/> <u>4014006</u>	March 1977	Sorensen et al.	
<input type="checkbox"/> <u>4947373</u>	August 1990	Yamaguchi et al.	
<input type="checkbox"/> <u>5006980</u>	April 1991	Sanders et al.	
<input type="checkbox"/> <u>5463582</u>	October 1995	Kobayashi et al.	
<input type="checkbox"/> <u>6026050</u>	February 2000	Baker et al.	
<input type="checkbox"/> <u>6166942</u>	December 2000	Vo et al.	

ART-UNIT: 2181

PRIMARY-EXAMINER: Ray; Gopal C.

ATTY-AGENT-FIRM: Fletcher Yoder

ABSTRACT:

A method and apparatus for reducing the number of data read lines needed in a memory device. Specifically, multiple helper flip-flops are used to prefetch data in a memory device. The helper flip-flops are configured to latch one or two of the data bits from a 4-bit prefetch in an alternating periodic fashion, thereby necessitating fewer data lines.

18 Claims, 7 Drawing figures

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